FIG. 1

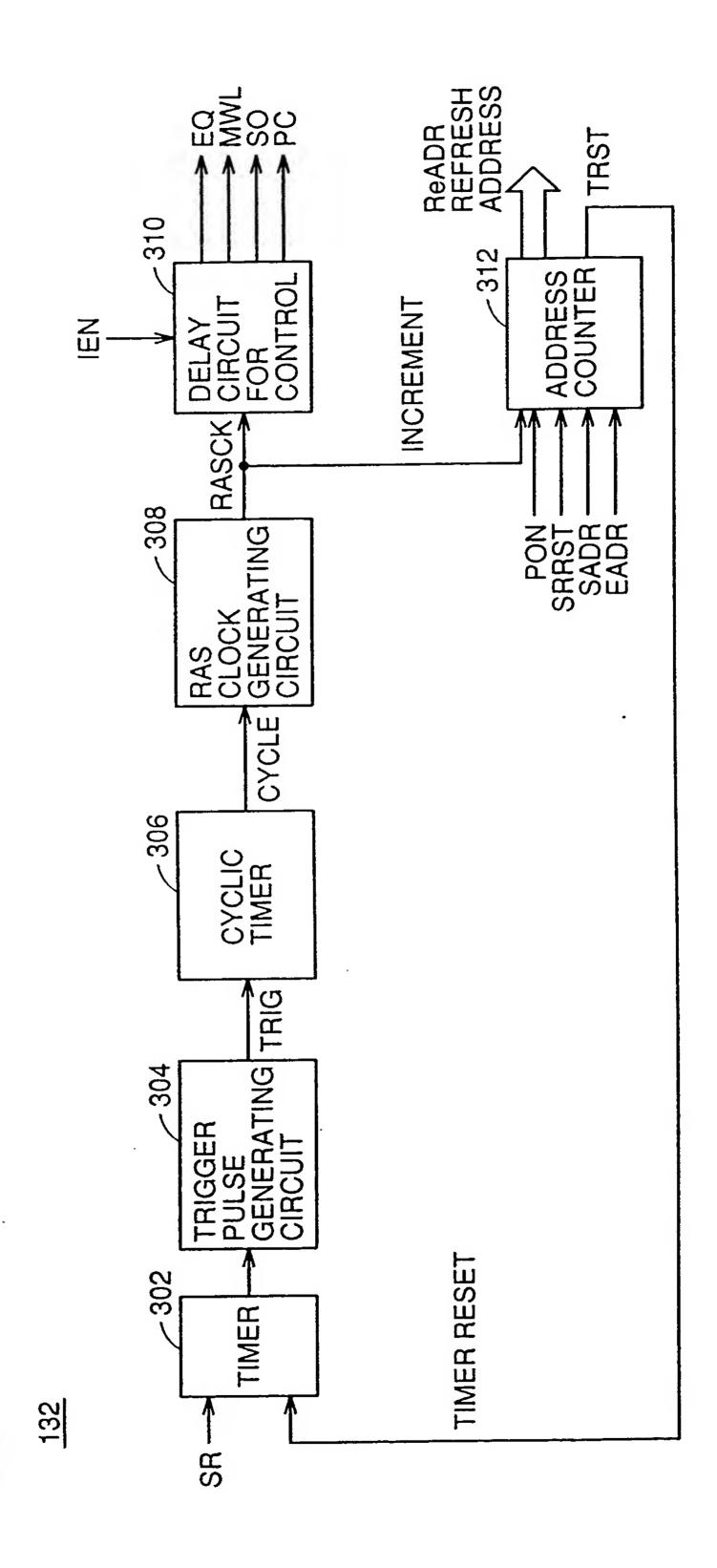


FIG.3

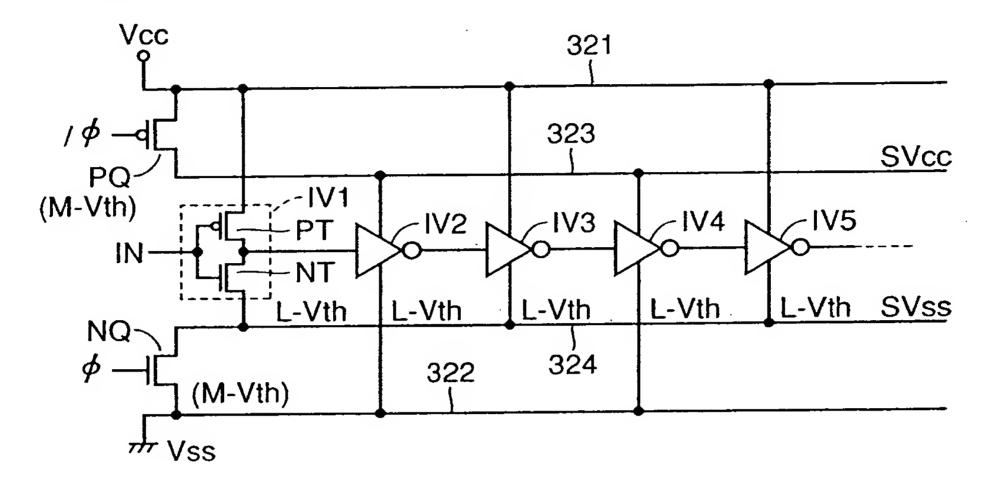
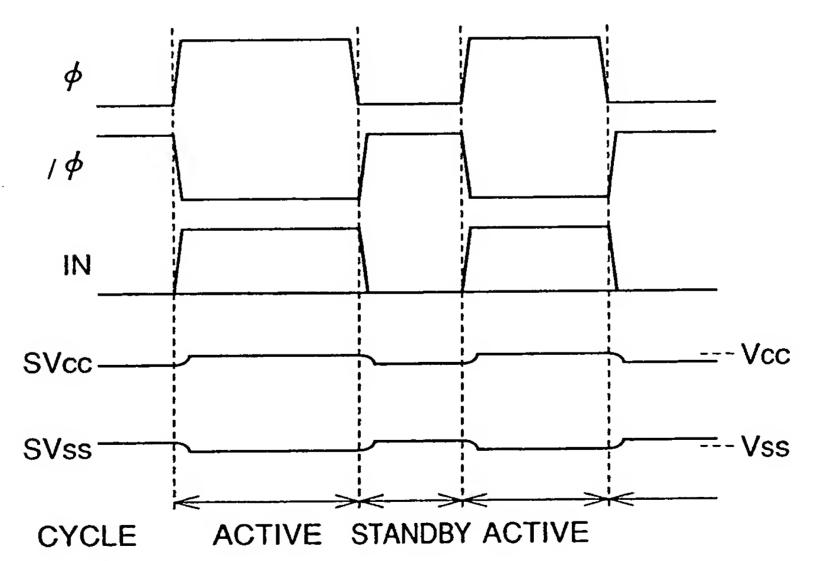
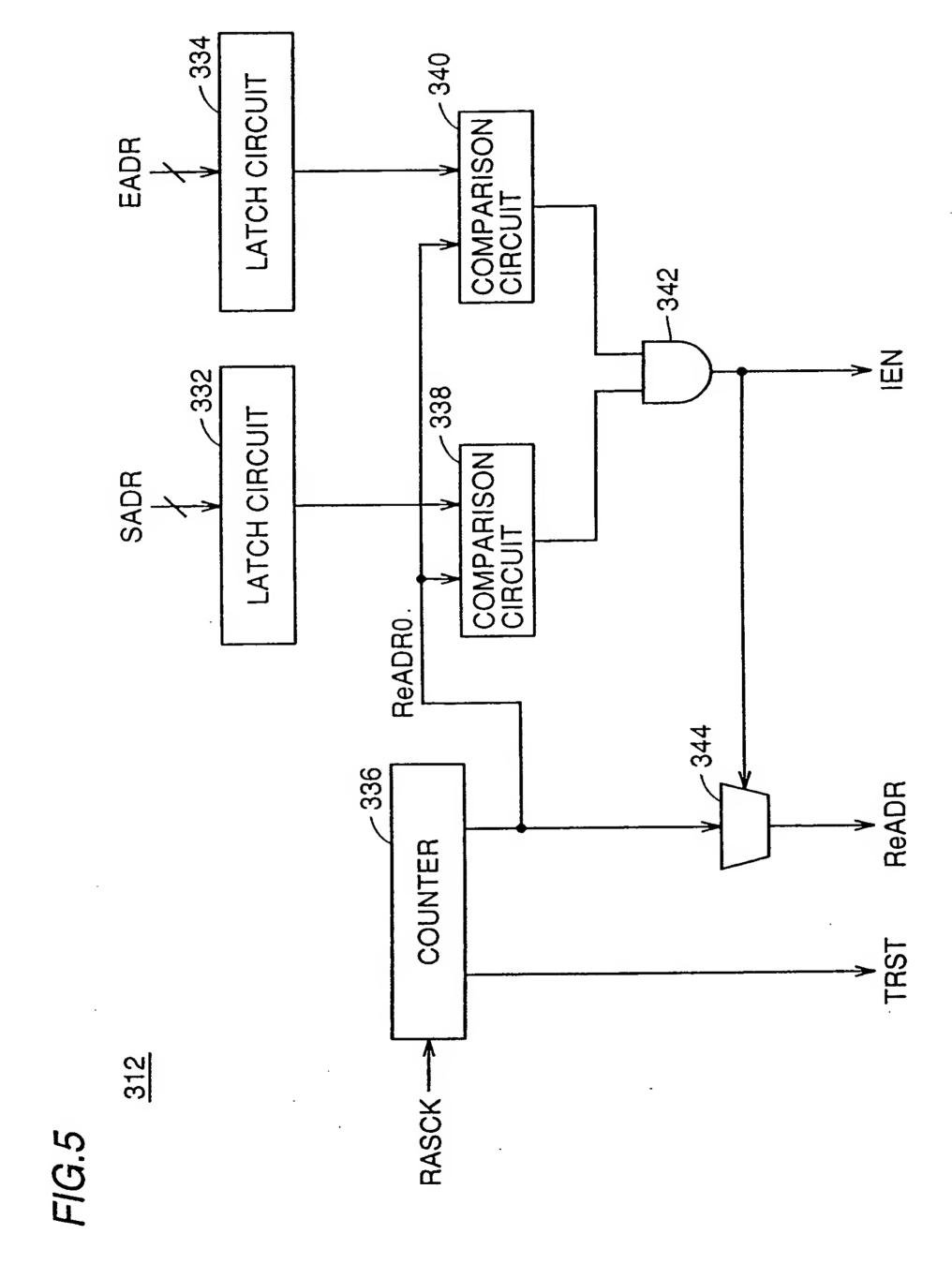


FIG.4





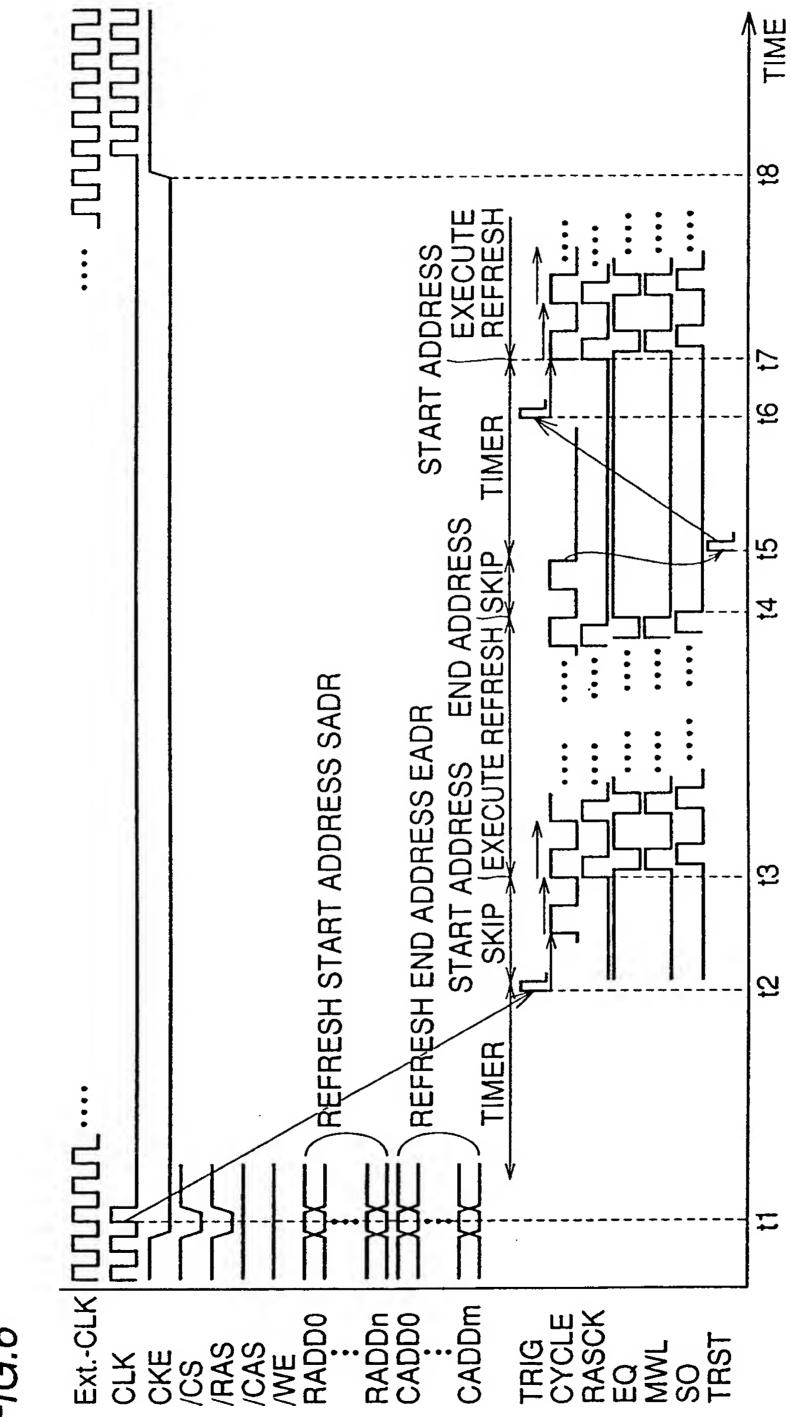
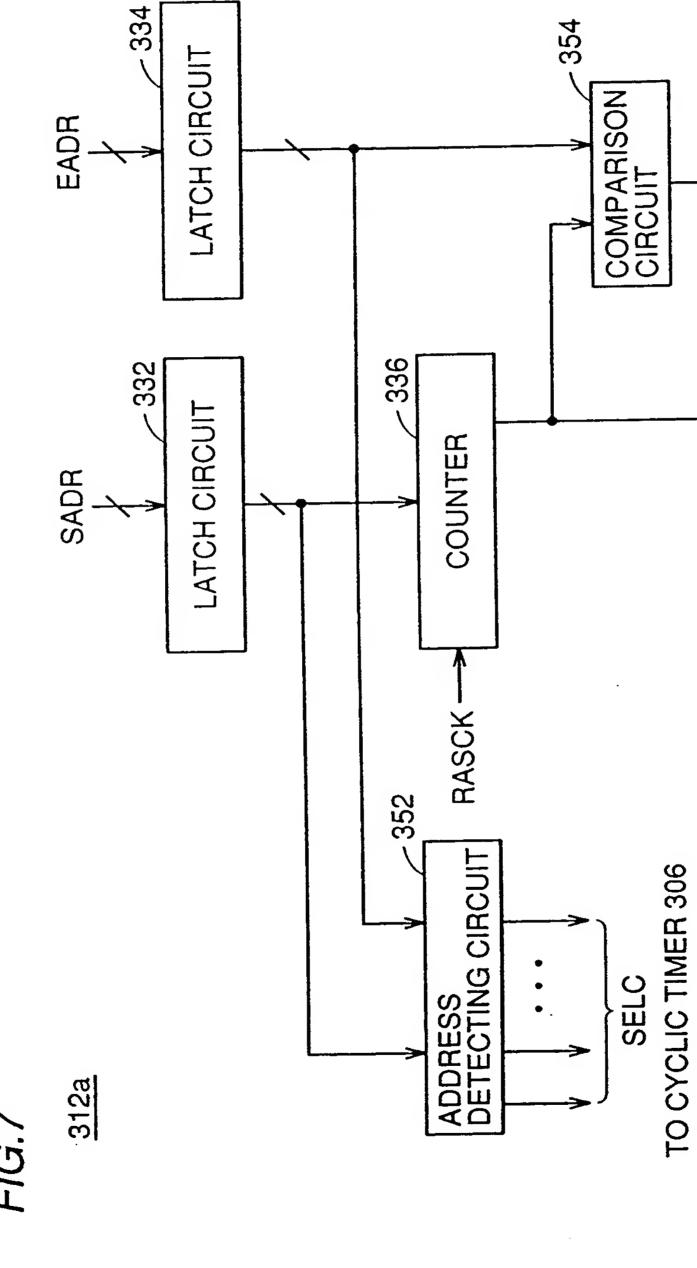


FIG 6



TRST

ReADR

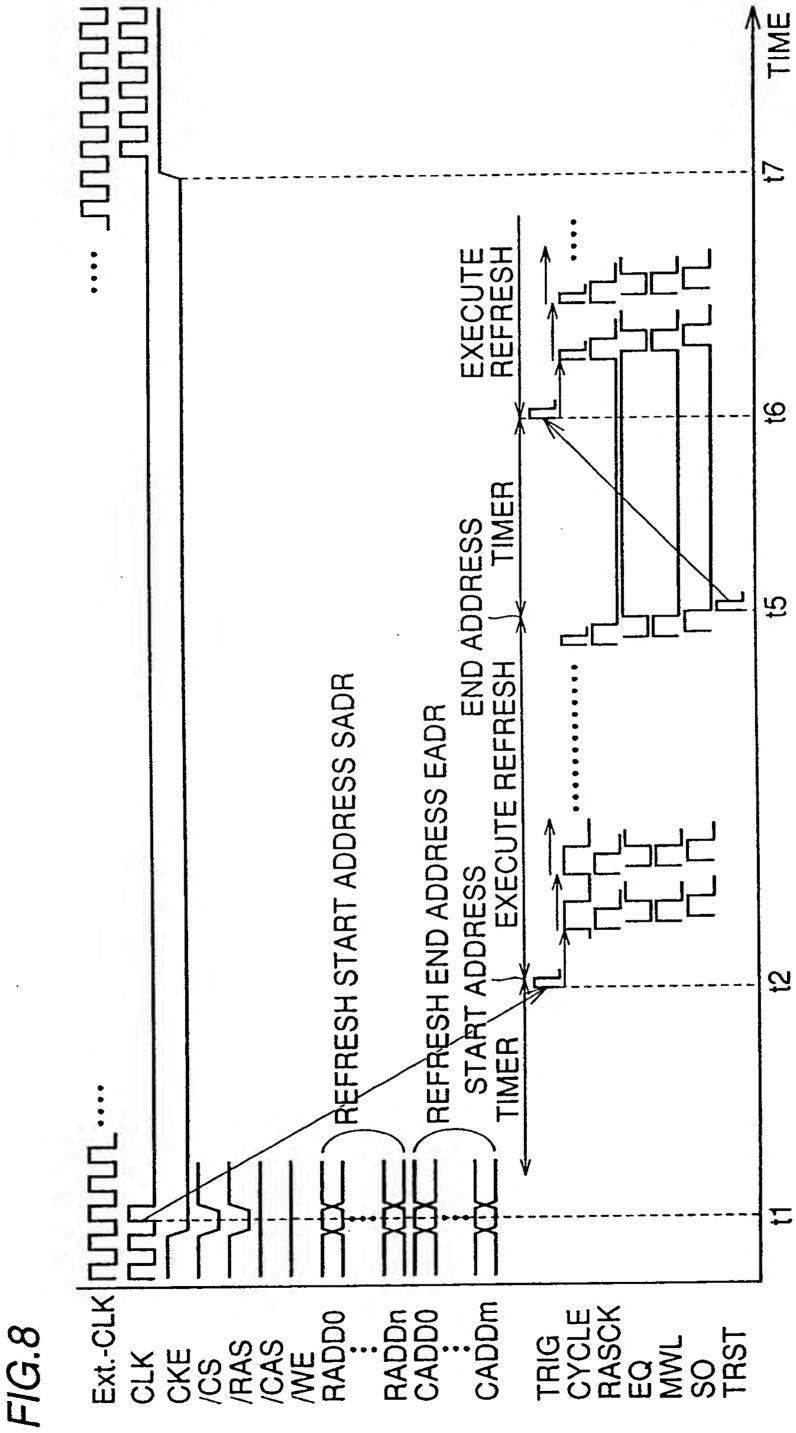


FIG.9

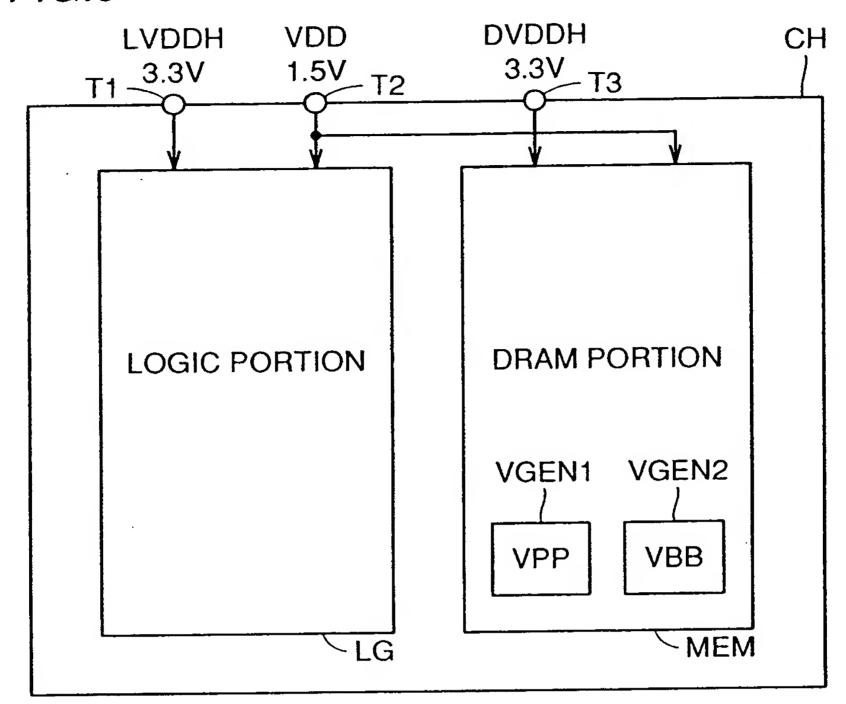


FIG.10 L1 ARY1 SW1 PCKT1 Tr1 < /SR PERIPHERAL **MEMORY ARRAY CIRCUIT** -SE1 7 2.0V L2 ≺ SR PCKT2 → DVDDH (3.3V) Tr2 VDD3 **VDC** PERIPHERAL CIRCUIT VDD3 Tr3 < SR L3 **⋬**2.0V¦ -SE2 **MEMORY ARRAY** < /SR Tr4 **VDD** ARY2 SW2 L4

FIG.11

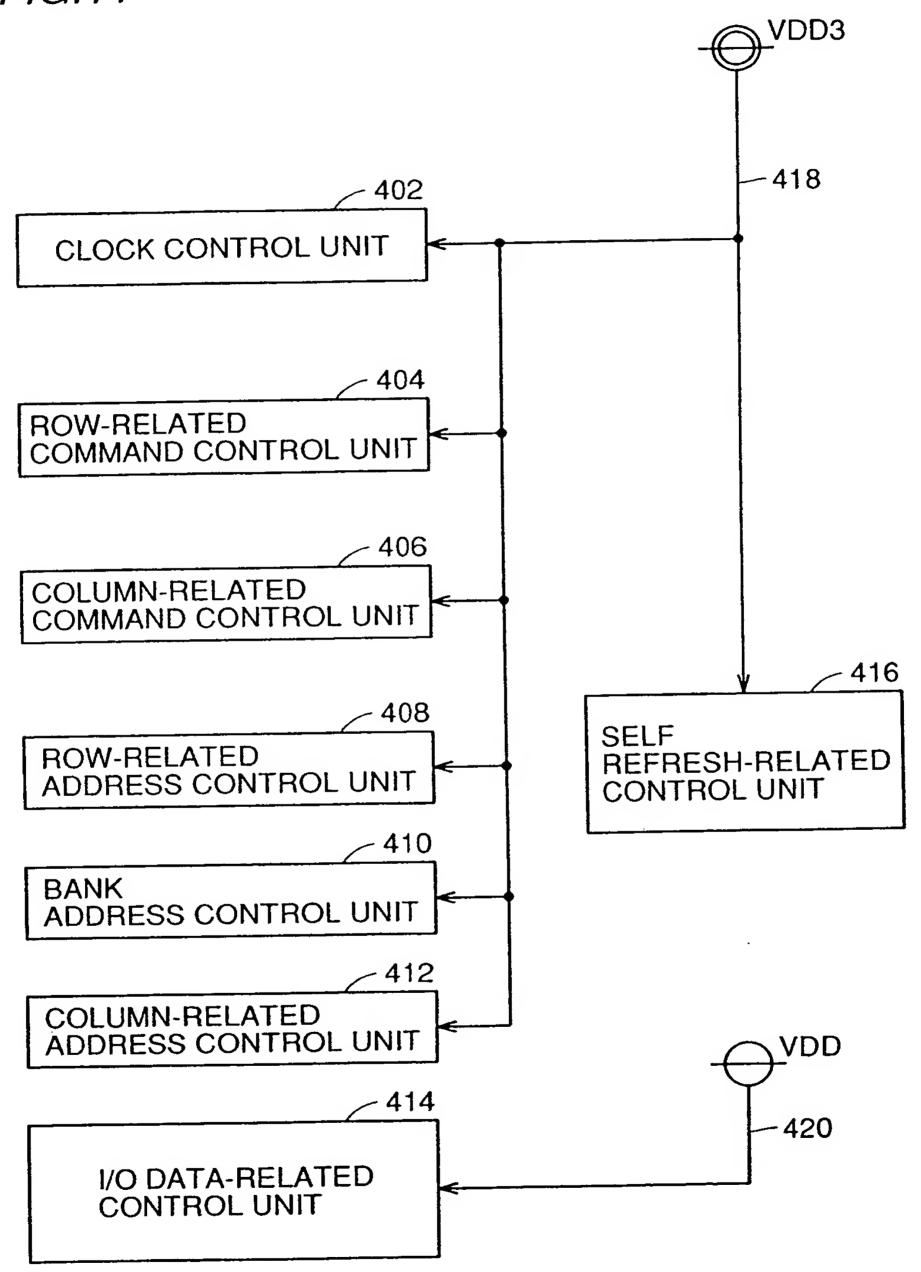


FIG.12

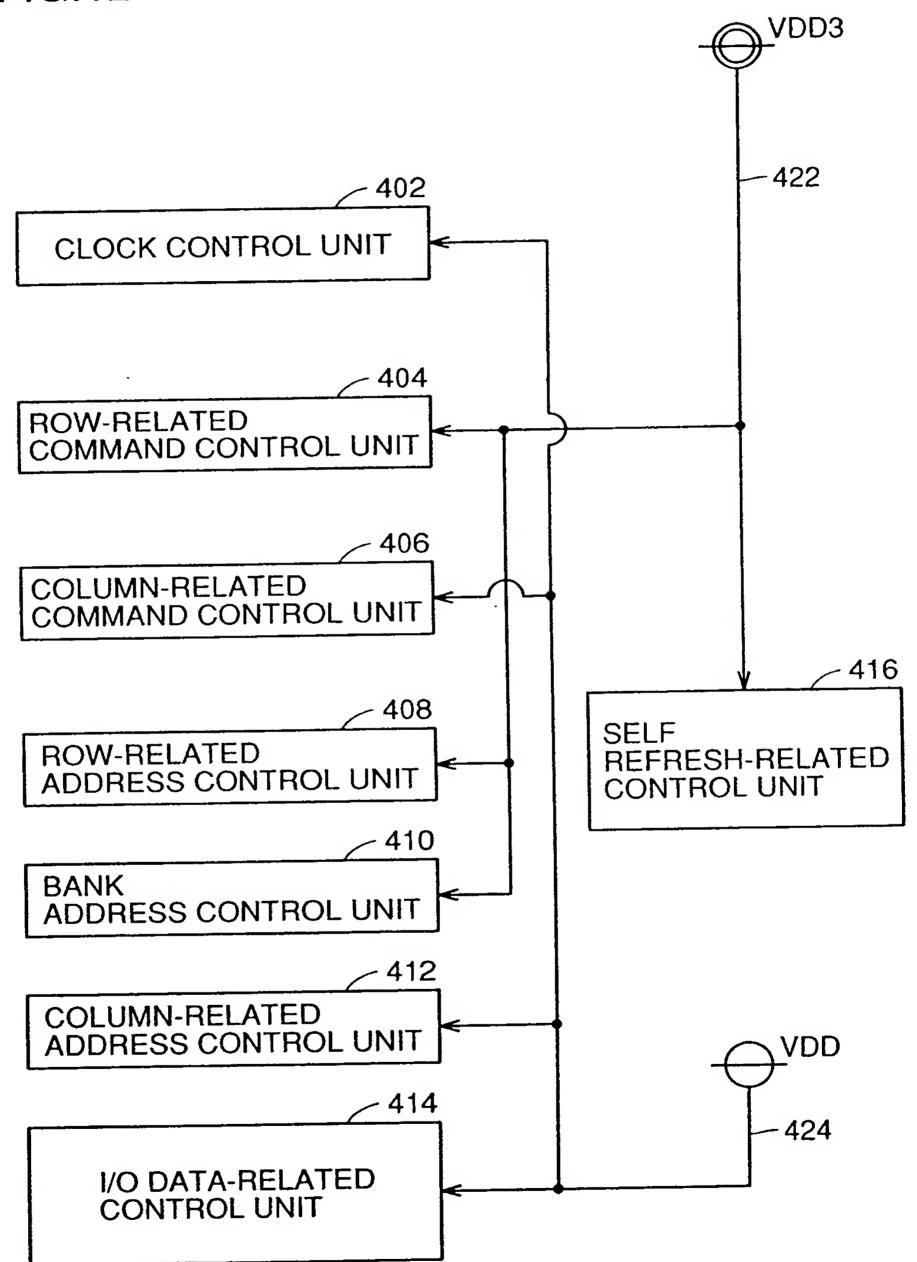


FIG.13

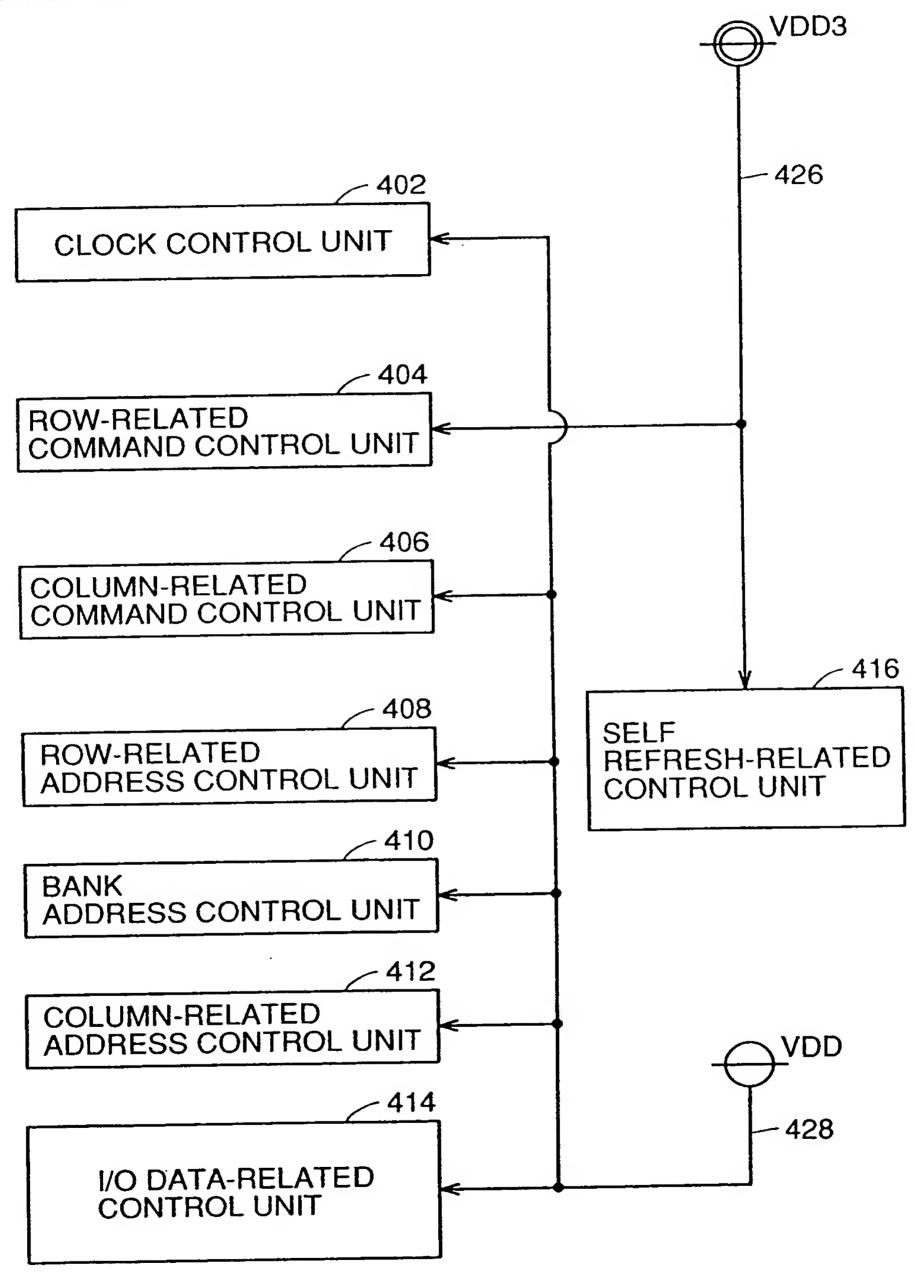


FIG. 14

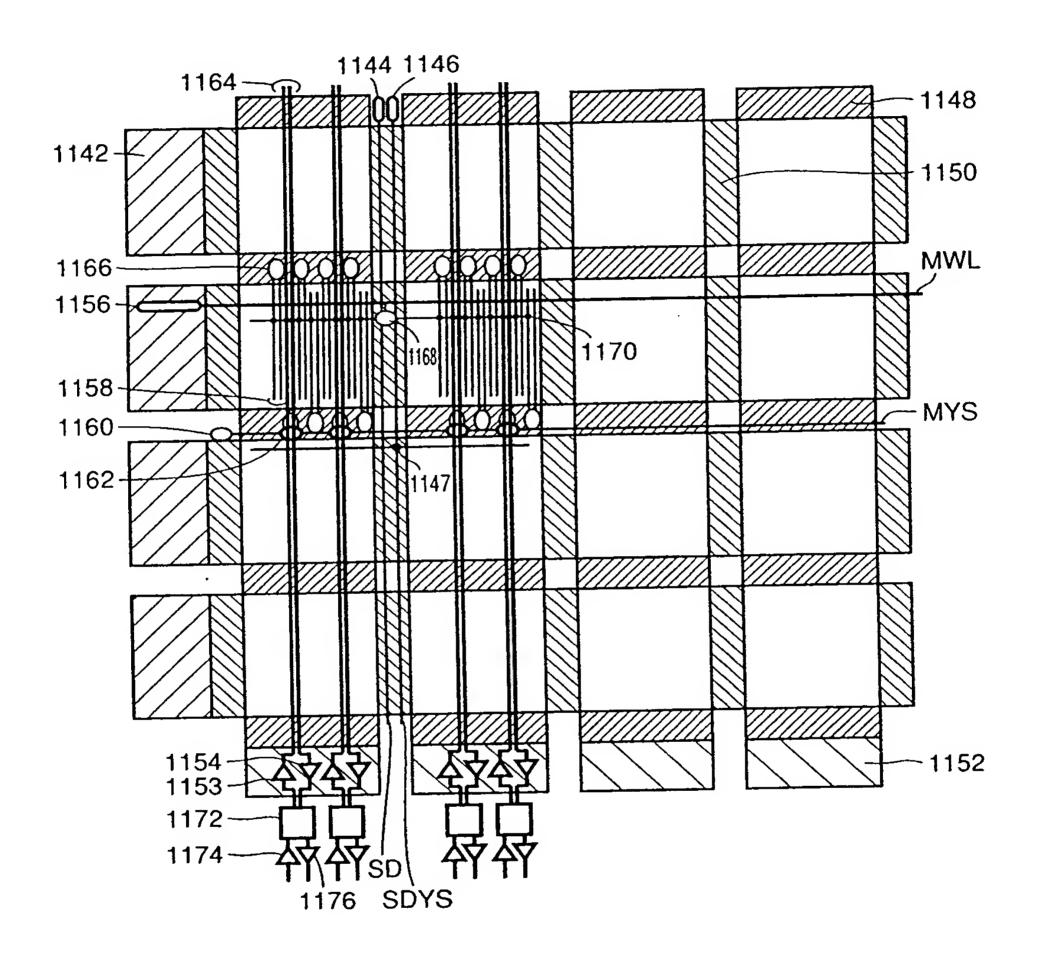


FIG. 15

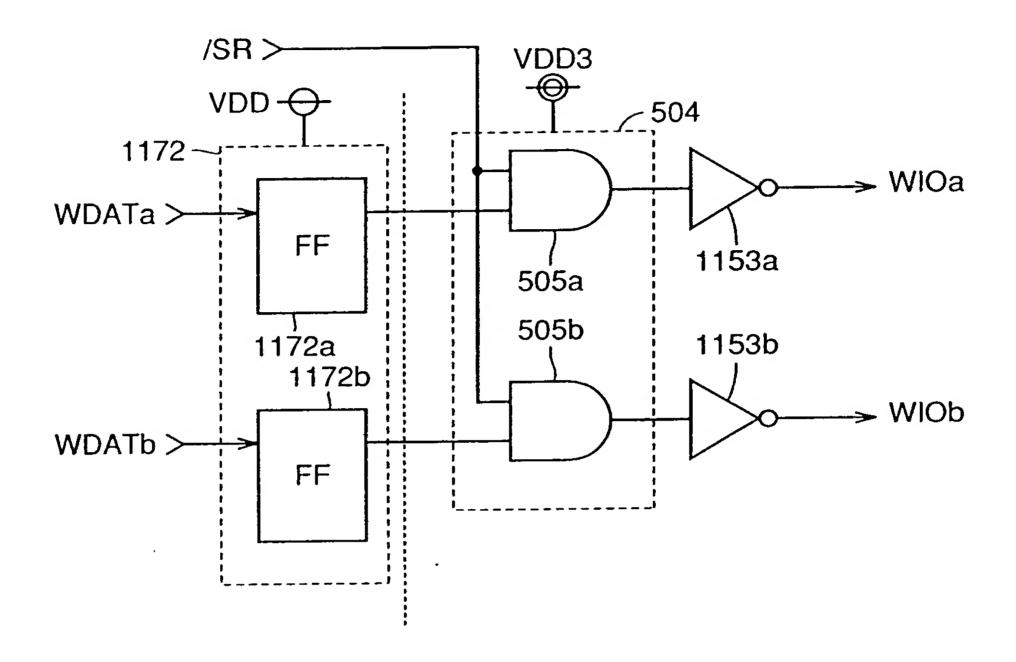


FIG. 16

FIG.17

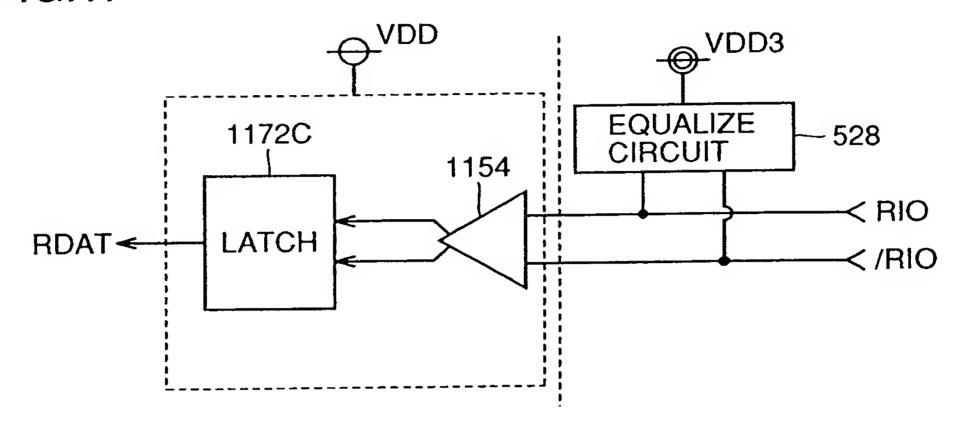


FIG.18

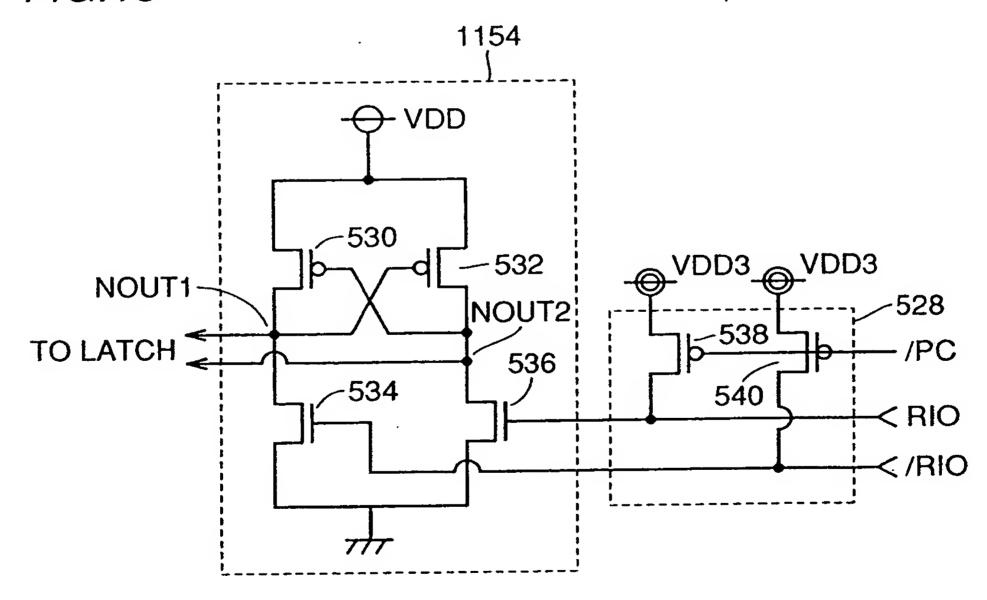
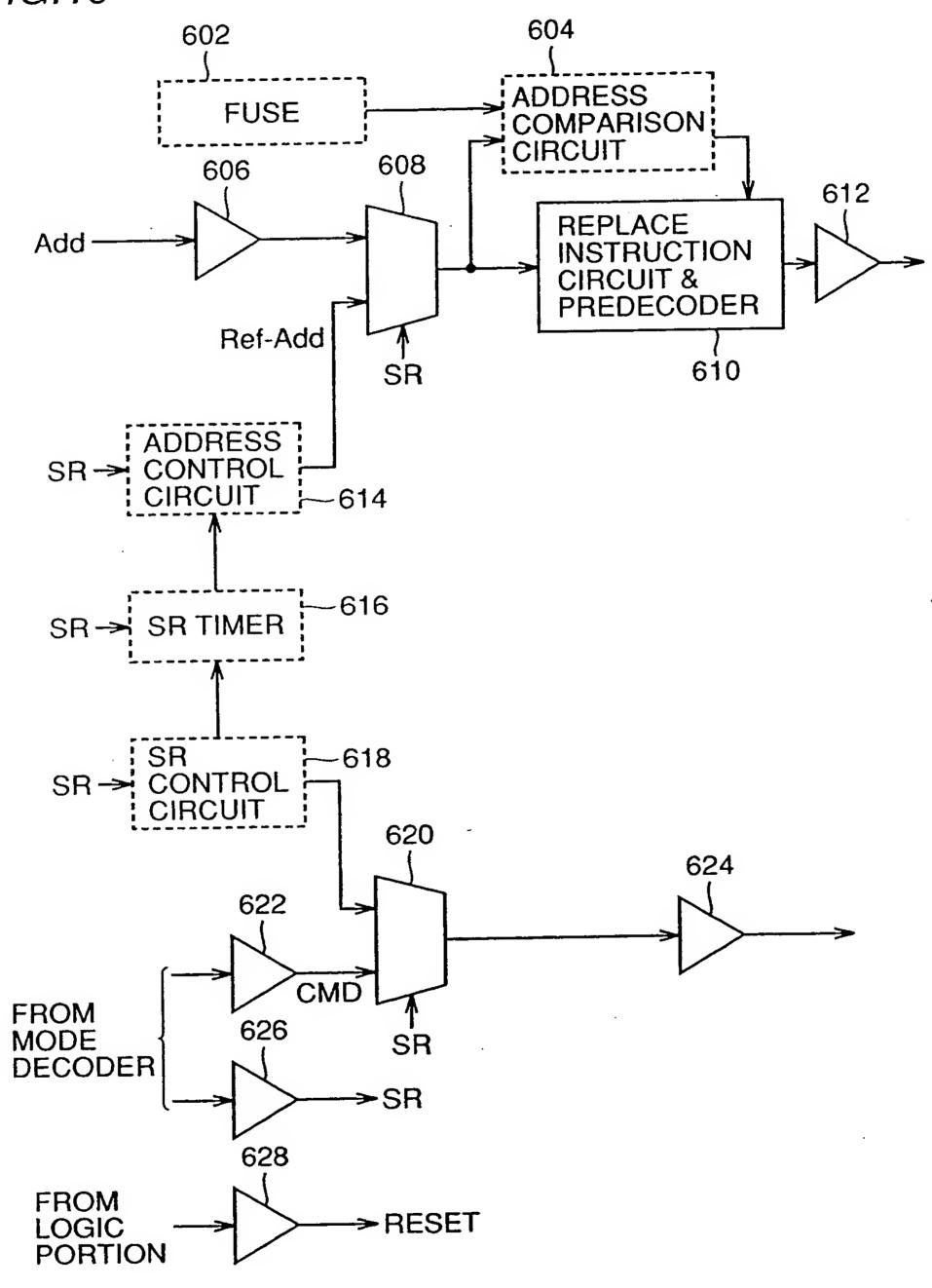
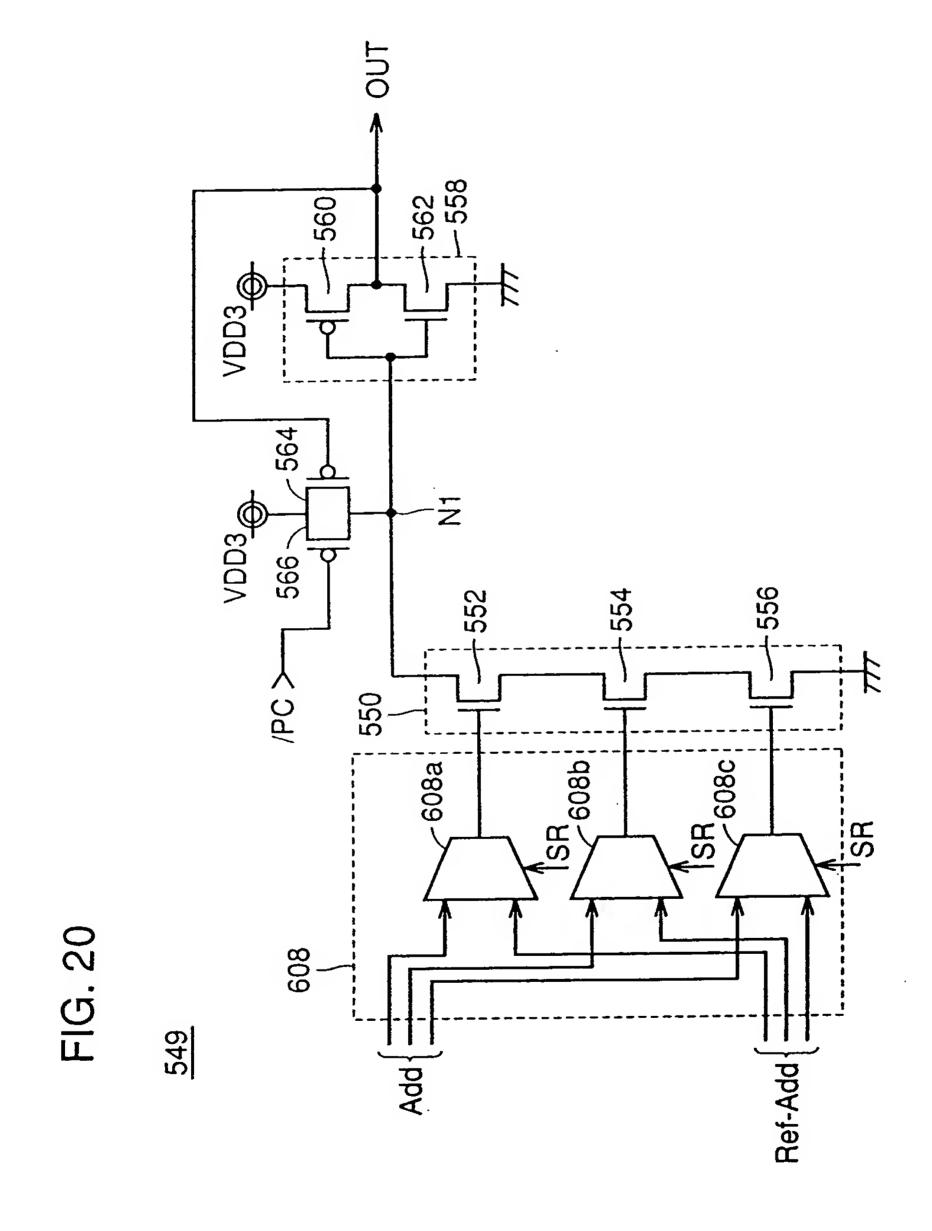


FIG.19





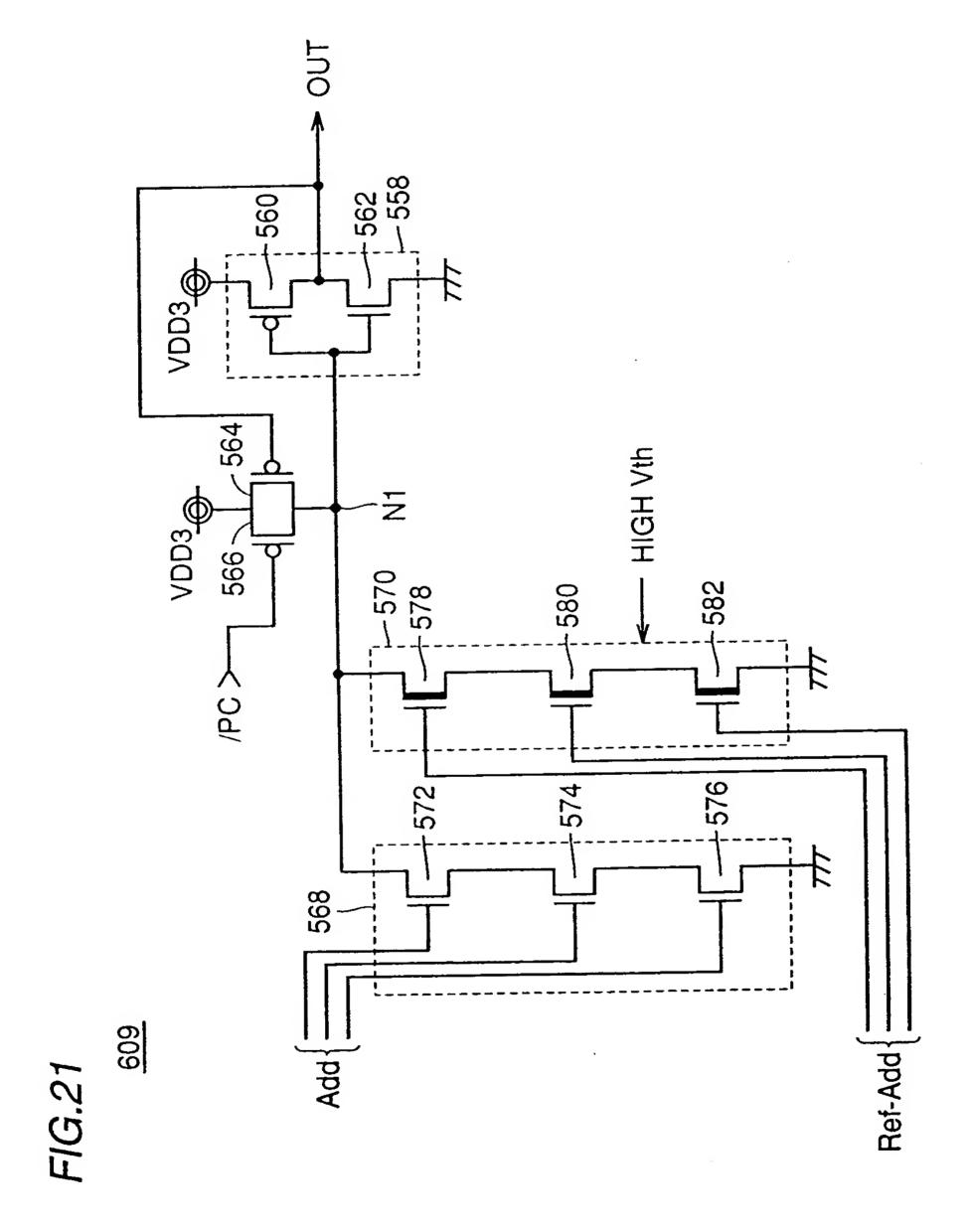


FIG.22

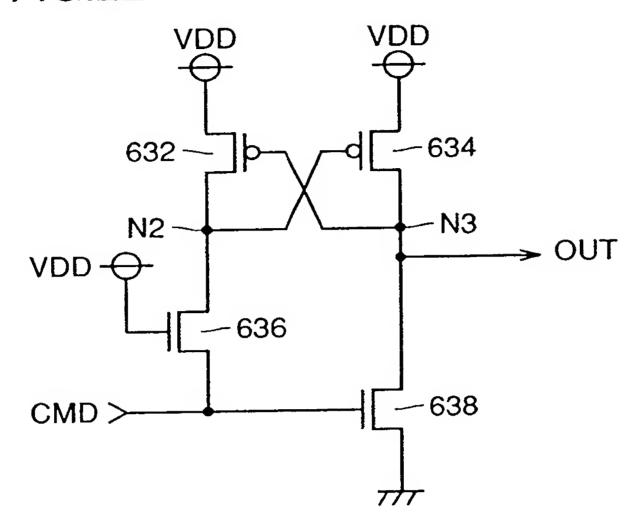


FIG.23

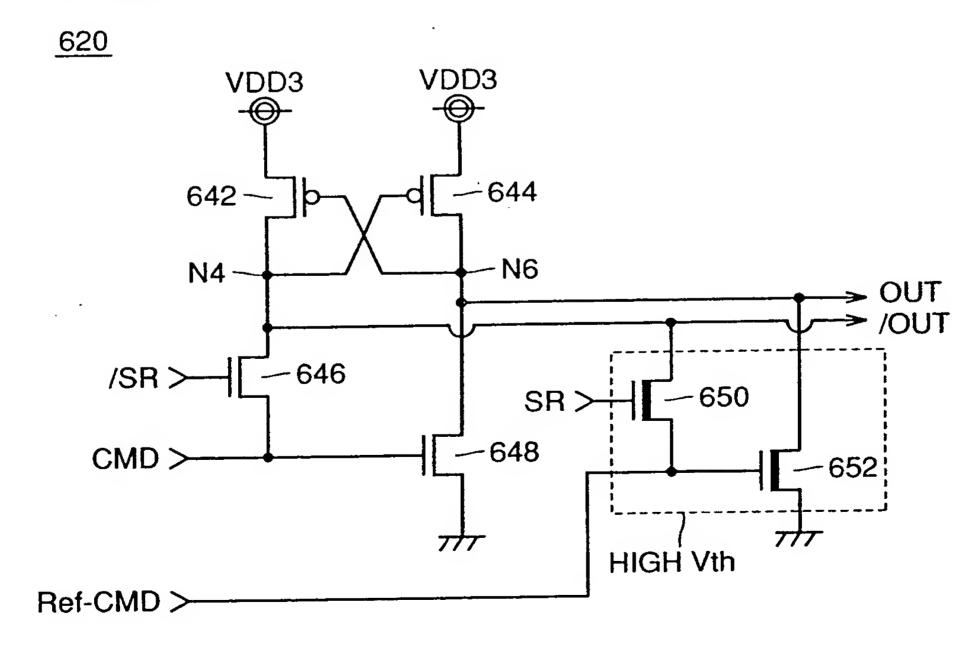


FIG. 24

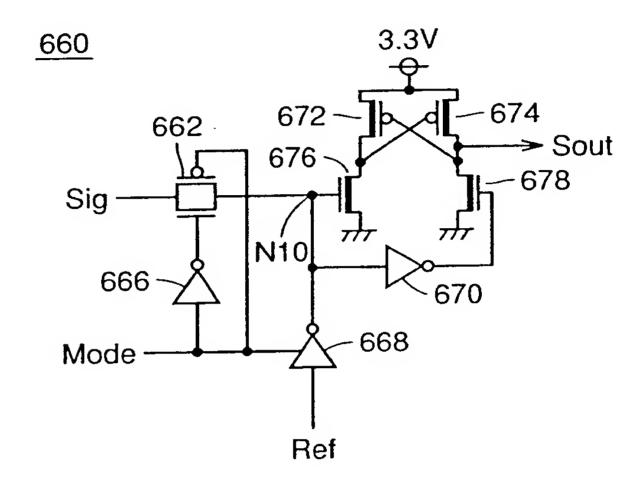


FIG. 25

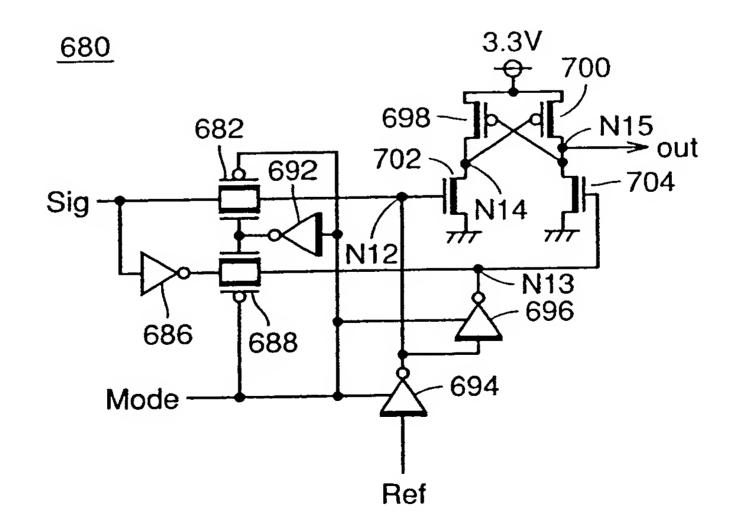


FIG. 26

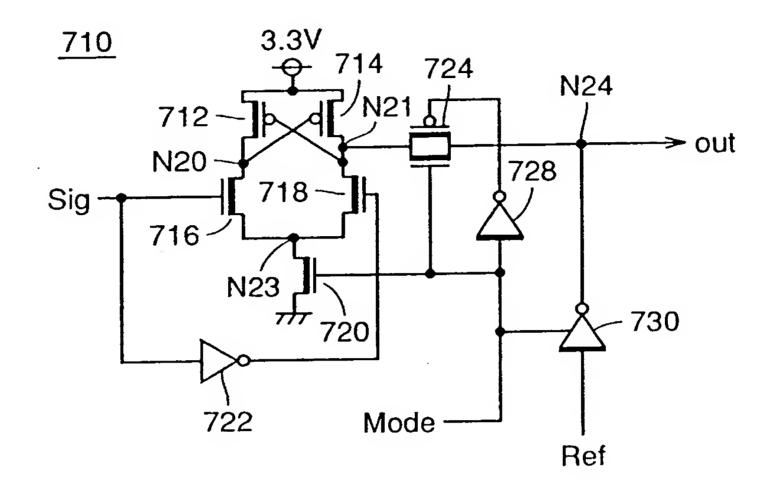


FIG. 27

<u>730</u>

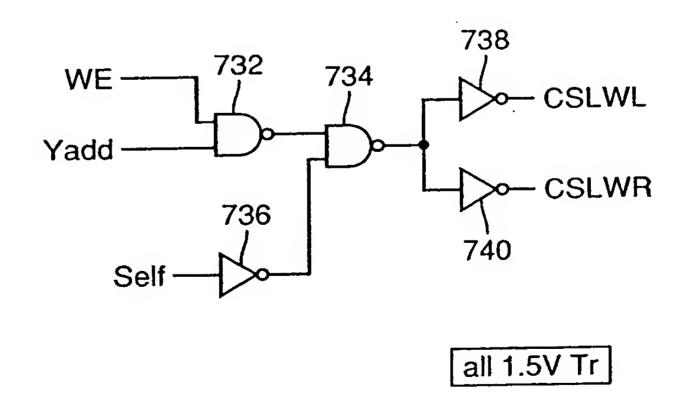


FIG.28

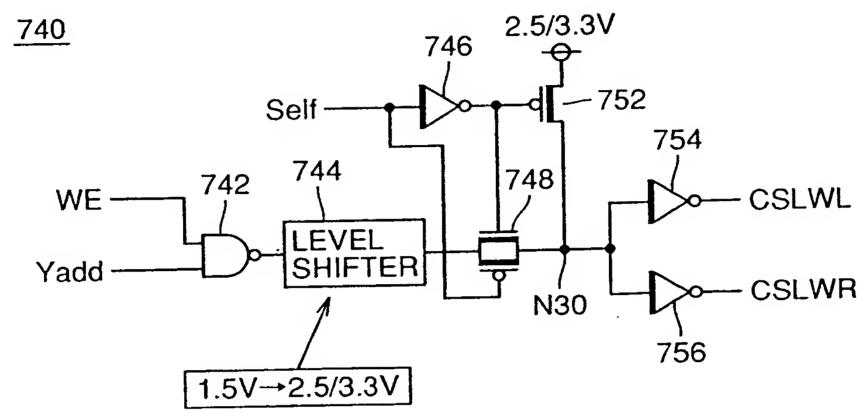
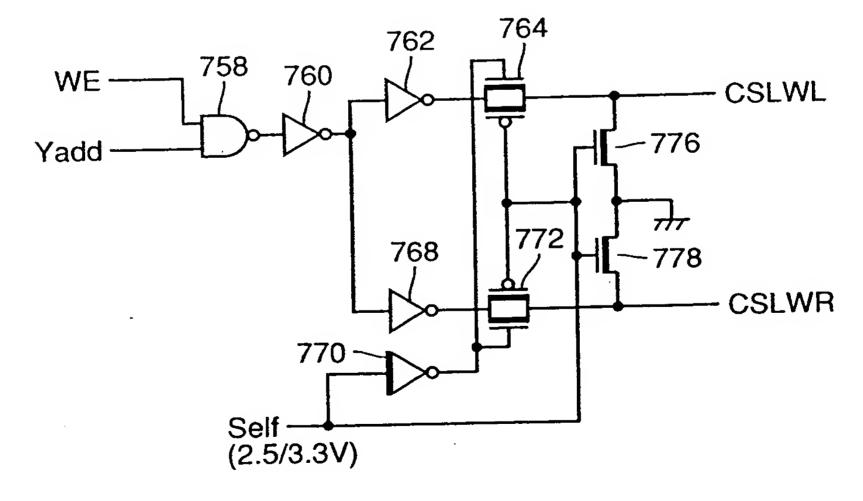


FIG.29

<u>757</u>



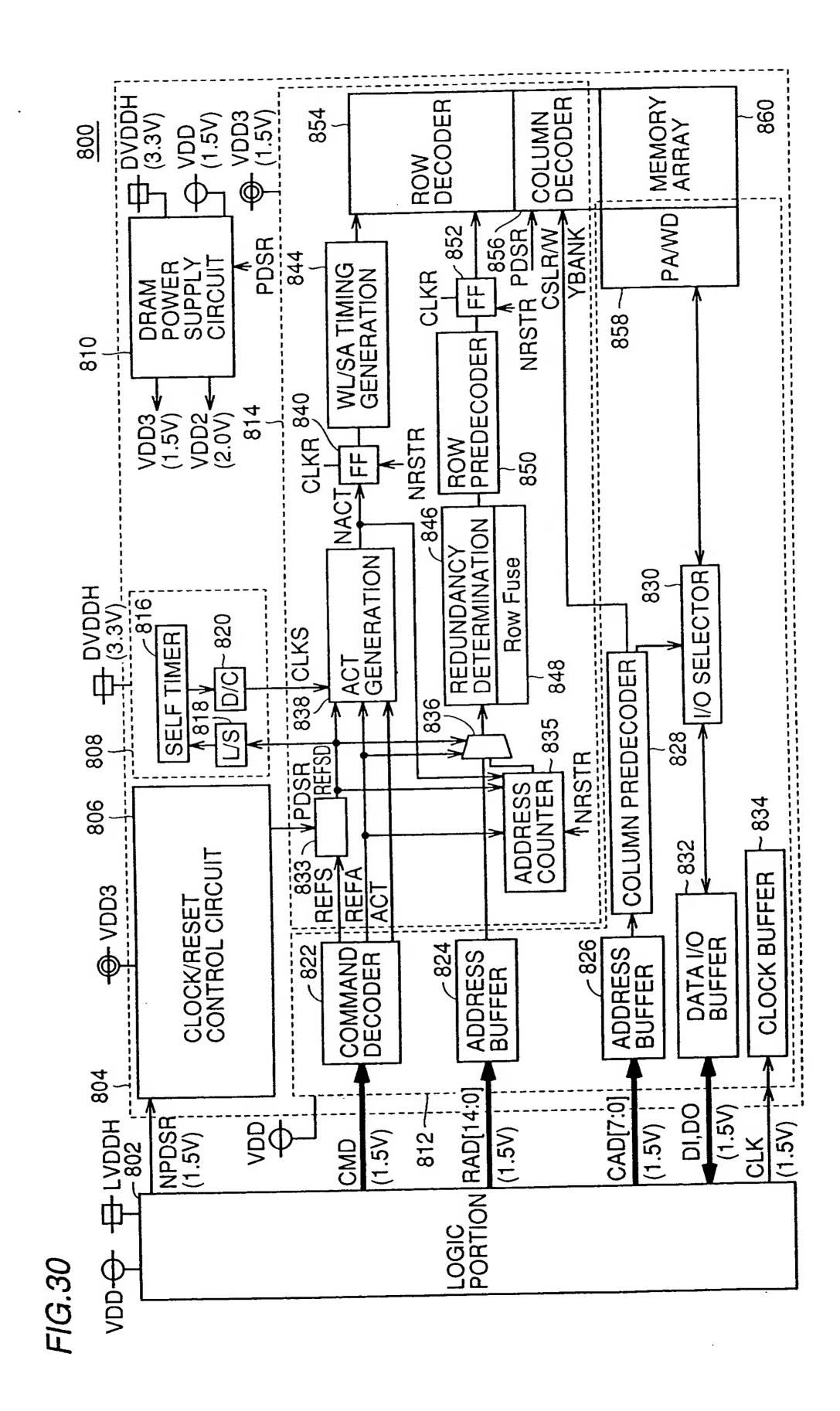
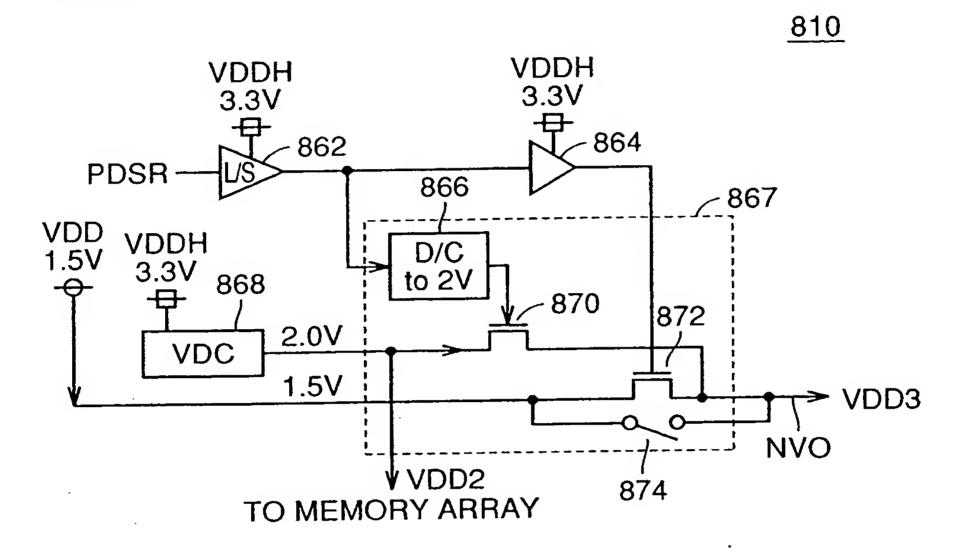
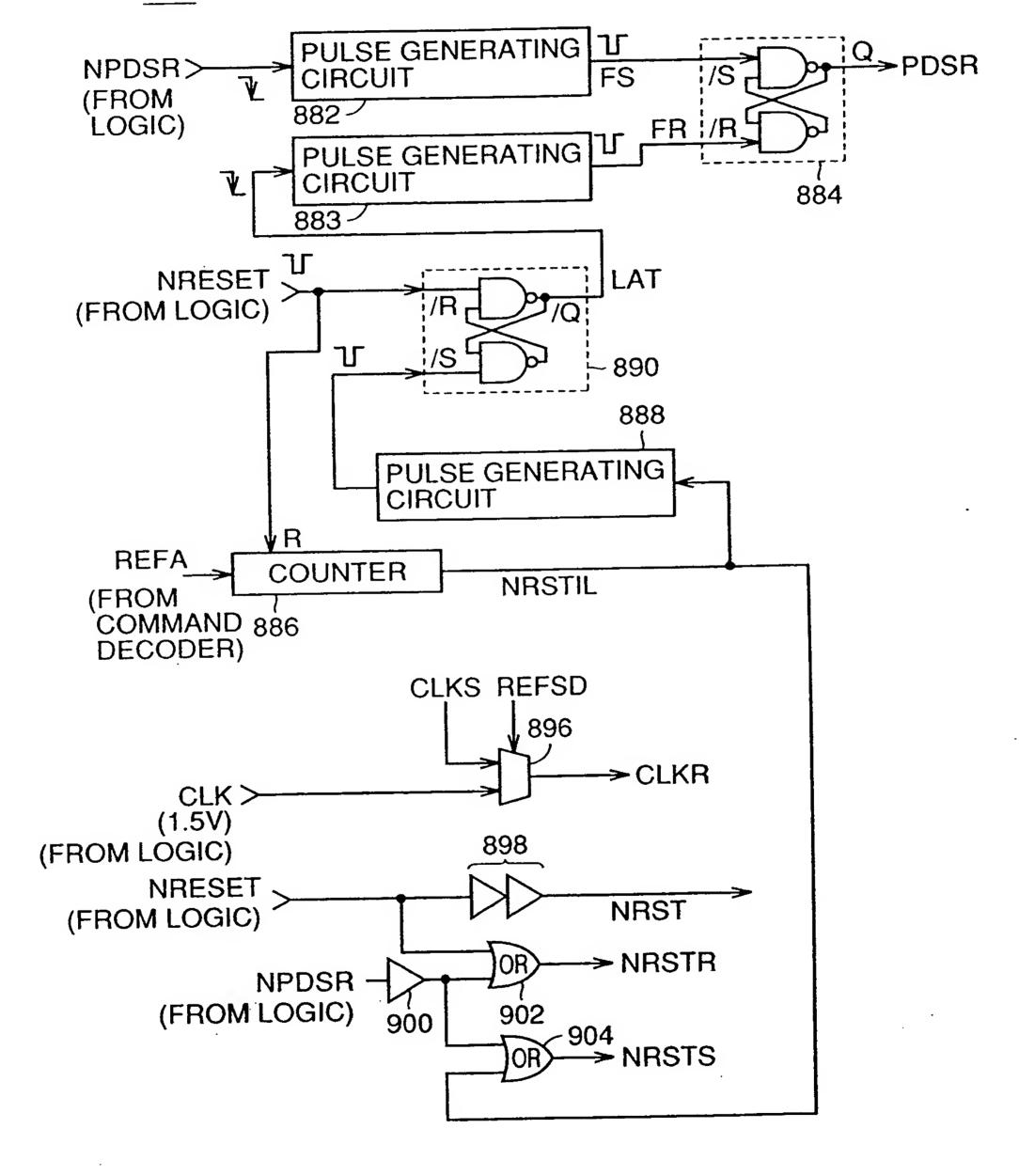


FIG.31



806



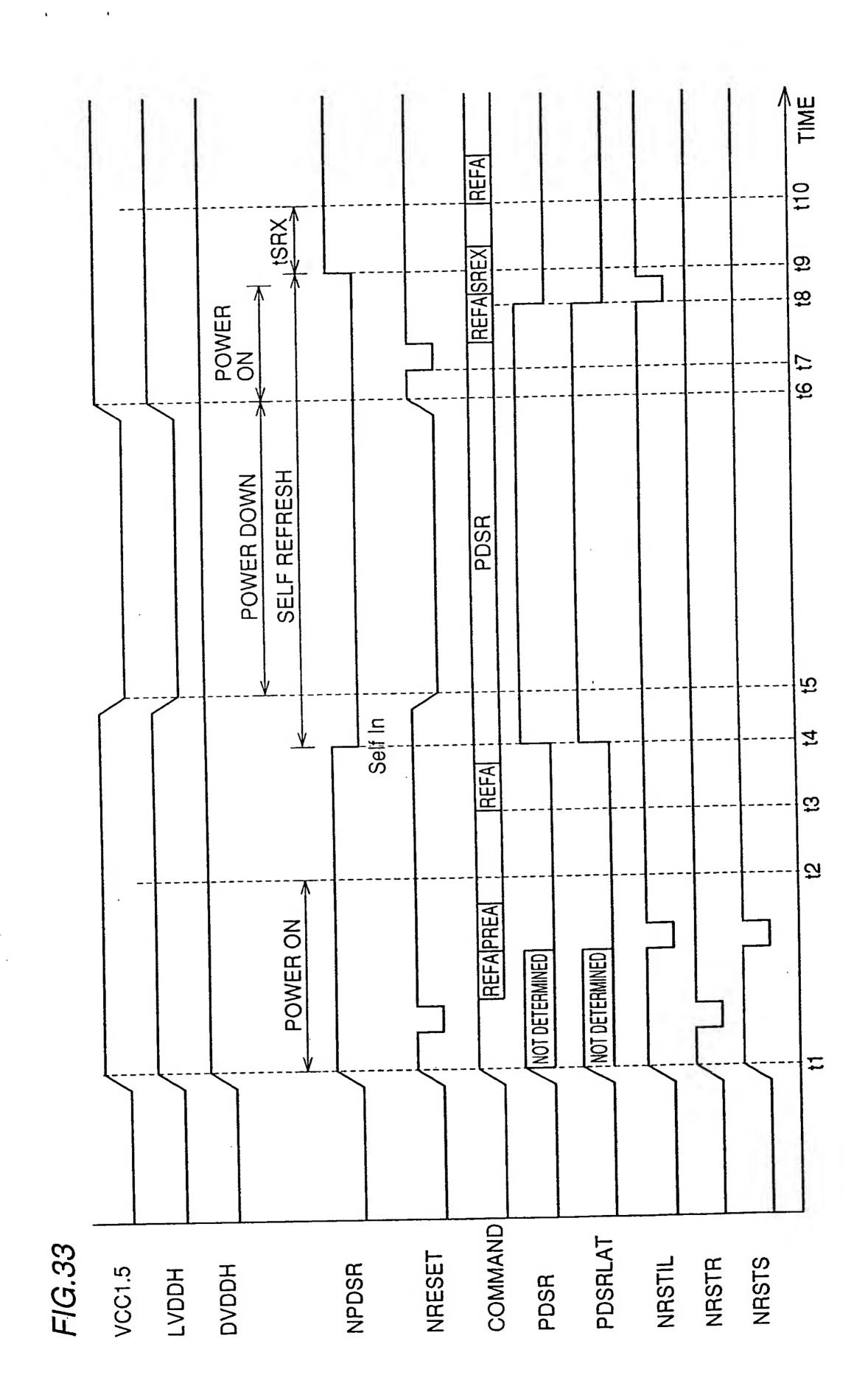
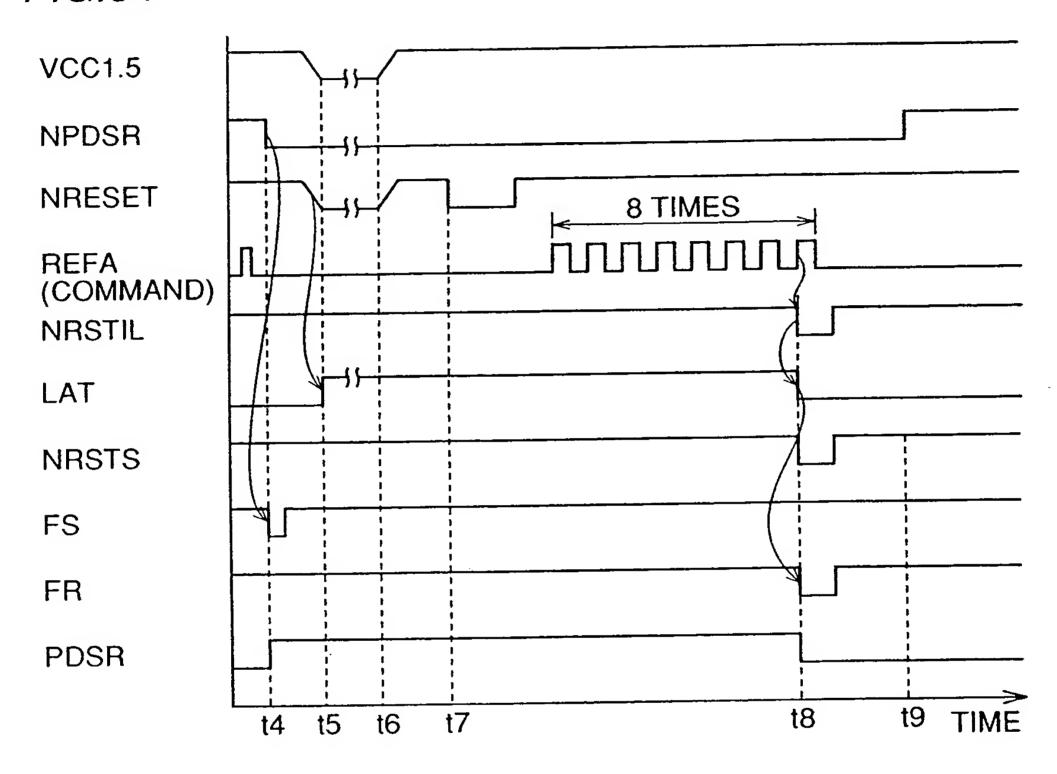


FIG.34



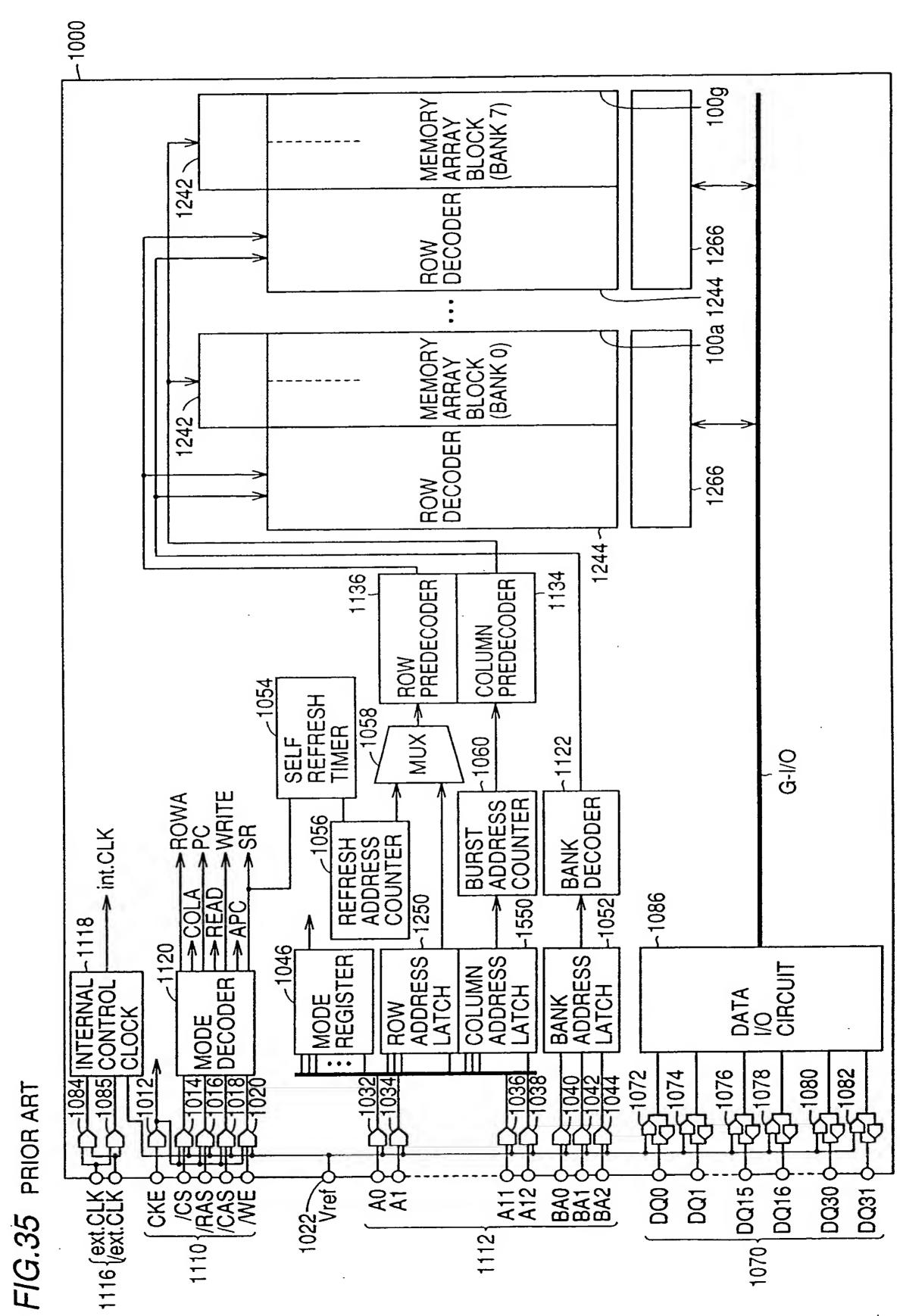


FIG.35

FIG.36 PRIOR ART

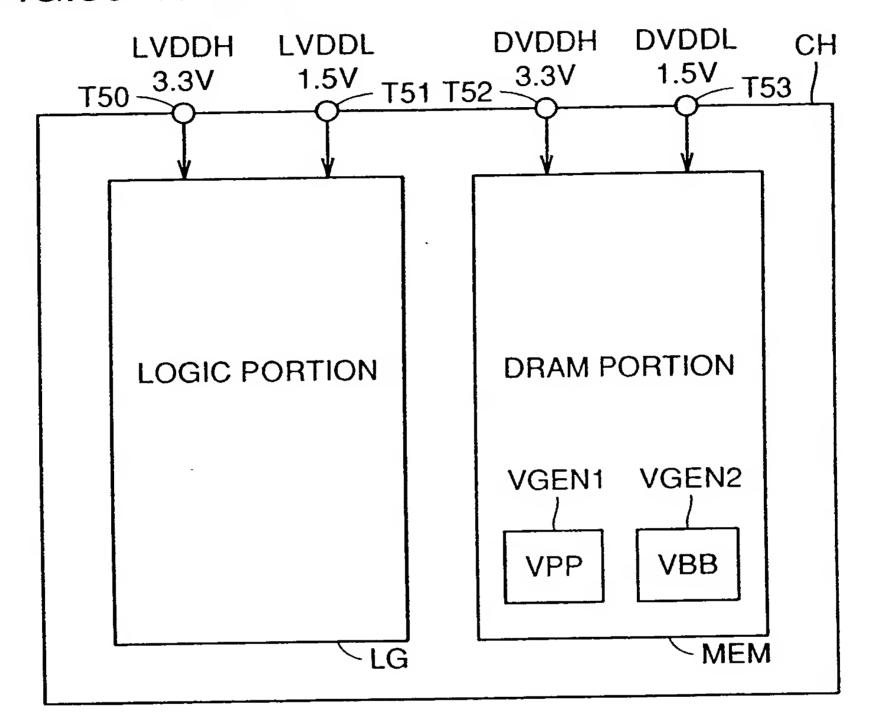


FIG.37 PRIOR ART

